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DATA ENCODING AND DECODING SCHEMES FOR NETWORK-ON-CHIP APPLICATION

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KEYWORDS: Network on Chip, Data encoding, coupling capacitance, accuracy.

ABSTRACT
The data encoding and decoding schemes are used to reduce the power dissipation of the communication system in a Network-on-Chip (NoC). A NoC comprises routers and interconnections allowing communication between the PEs.The self-switching and coupling-switching actions are caused for link power dissipation. The end to end basis have been proposed data encoding and decoding schemes are mainly working at flit level ;which allows us to reduce the both self and coupling switching activities. The scheme uses the binary to gray translation at the transmitter and gray to binary translation at the receiver. The self-switching is reducing by checking the switching transition and then the coupling system is included with the wormhole routed network. The proposed scheme has maximum power consumed is 2.2mW the design of encoder and decoder architecture the performance in various kind of scheme have to be analyzed and to obtain the end to end scheme.

INTRODUCTION
The Network on chip is a promising approach for the execution of on chip announcement architecture. The system on chip designs incorporating large number of processing cores and modular structure of Network on chip makes a fitting surrogate for system on chip. Network on chip is proposed to solve the shortcomings, by implementing a communication network of switch, micro routers and resources. System on chips are not containing IP cores only and conventional methods for communication such as bus are not fit solution for future System on chips. The Network-on-Chip has emerged as essential infrastructure for communication between IP cores. Network on chip is solution for communication architecture of future SoC that are composed of switches and IP cores where communicate among each other through switches. Between IP cores data move in the form the packets. As the technology shrinks the power ratio between link and router increase making link more power starving than routers. A network on chip communication gives flexibility in the topology, in support to that the flow controls. A routing algorithm, self switching techniques guarantying the quality of service. Network on chip is come near to design the communication subsystem between intellectual property cores in a system on chip. The communication approach in system on chip uses dedicated buses between communicating resources. Another chance is the use of common buses, which have the problem that it does not scale very well, as the number of resources grows.

Network on chip is a communication subsystem an on integrated circuit typical between IP cores in a system on a chip. NOC technology applied methods to on chip communication and brings notable improvement over straight bus and crossbar interconnections. NOC improves the scalability of SOCs and the power efficiency of complex SOC, compared to other designs. A network on chip uses packets to transfer data between IP core interfaces within a chip.The NOC based system on chips imposes different design issues on the fabrication of such integrated chips. Firstly, the suitable topology for the target NOCs such that the giving supplies and design constraints are satisfied. Secondly, the design of network interfaces to access the on chip network and routers provide the physical interconnection mechanisms to transport data between processing cores.

Finally, as technology scales and switching speed increases, future network on chips will become more responsive and prone to errors and faults. On-chip communication problems are more relevant to compare to the computational relevant problems. The header flit, the encoder encodes the outgoing flits of the packet such that the power dissipated by the inter-router point-to-point link

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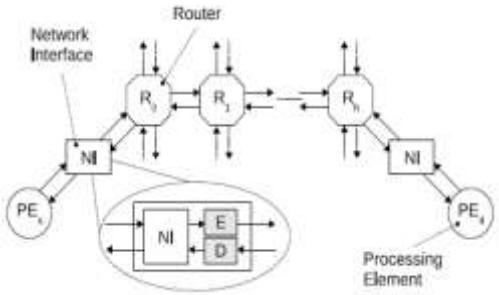

Fig1. General scheme of the proposed approach

In this paper techniques meant at reducing the power dissipated by the network links. In power dissipated by the network links is as relevant as that dissolute by routers and network interfaces (NIs) and their input is expected to increase as technology scales. In this work, we are going to falling the power indulgence in the network links. The power dissipation in the network on chip is applicable to the power dissipation in the routers and Network Interfaces (NIs). The power spending in a NOC grows linearly by increasing the total bit transitions in consequential data packets sent through the interconnect architecture. By using the switching activity are reducing by the coding schemes on both wires and logic in this system dropping the power consumption in the NOC. The power due to self-switching activity of entity bus lines while ignoring the power indulgence due to their coupling switching activity. Data encoding is mainly used for sinking the number of bit switch over interconnects. Adaptive coding, Bus invert (BI), Gray coding and changeover method these are the various encoding techniques used in the NOC. The data encoding with gray input is mainly falling the power dissipation on the NOC.

The number of IP modules in System-on-Chip increases, bus-based consistent architectures may check these systems to meet the show by more applications. For systems with serious parallel communication needs buses are not provide the needed latency, bandwidth, and power spending. To overcome such a announcement holdup is the use of switching network, called Network-on-chip. NoC is an on chip package based communication system between blocks linked via routers. In current years research has shown that Network-on-Chip is likely to replace buses. Network-on-Chip architectures maturity comes directly from the improving the distress around System-on- Chip and Multi-Processor-System-on-Chip technologies. The designing thinking leaning to the concept of MPSoC is even more up-to-date and absolutely ropes engineers to study and to develop the be linked technologies available present days. To known the supplies of the NoCs, it is useful to think the challenges faced by SoC and MPSoC. Technological modifications in the ground of silicon technology open the road for large presentation improvements. Regrettably these technological improvements to be fully broken needed a rethought of present VLSI design flow. There is a one possible solution to these problems needs a grave adoption of hardware reprocess methodologies that becomes the way to the making of fake platforms, while reducing the design effort for design a new systems. The improvement of the number of fundamentals that requires to be organized is starting to move up the negative side effects of classical “shared bus architectures, and presents the required for an interconnection of a system that allows the one IP to use the communication resources at a time. In particular, a set of data encoding and decoding schemes working at flit level and on an end-to-end basis, which allows us to reduce both the self and coupling switching actions on links of the steering paths traversed by the packets. The future data encoding and decoding schemes, which are apparent with respect to the router execution, are presented and discussed at both the architectural level and the algorithmic level. The investigation takes into account several aspects and metrics of the design, including power dissipation, silicon area, delay, and energy consumption.

RELATED WORKS AND CONTRIBUTIONS

The data encoding techniques for low power have been proposed in literature. Almost all of them have been defined to be functional in the context of bus-based architectures with the primary goal of minimizing transition activities on buses though ignoring cross-coupled capacitance. Bus-invert method can be applied to encode at

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random distributed data patterns. Highly correlated way in pattern exhibit spatiotemporal locality which is exploited by Gray code, T0 method and the working-zone encoding. Application specific approaches based on a priori knowledge of the traffic patterns have been proposed. Other encoding techniques have been defined to take into consideration the supply of cross-coupled capacitance. All the above proposals have been functional in the context of bus-based architectures. In the context of NoCs, evaluate the use of partial bus invert coding as link level low power encoding technique with the conclusion that it spends several times more power than no encoding at all, if normalized for the same performance, which is done by adjusting supply voltage and frequency, they consider point-to-point encoding in which every router in the NoC decodes the incoming flits and encodes the outgoing flits. In addition does not take benefit of the pipelined nature of the flow of flits through the links of the steering path which is guaranteed by the wormhole switching technique generally used in NoCs. The data encoding scheme that will be presented in the following is designed to exploit the wormhole switching technique creation it possible to operate an end-to-end encoding which does not resolve any
Overhead in terms of routers and links. It only requires the improve of the network interface which is enhanced with the encoding decoding logic leaving the underling network.

The general scheme of the proposed advance is depicted in Fig. 1. The basic idea is to fear an encoding technique end-to-end attractive advantage of the wormhole switching technique. In fact, wormhole switching is the most suitable option for on-chip statement .The basis behind this idea is due to the pipeline nature of wormhole switching. Since all the relations of the routing path are traversed by the same sequence of flits, the encoding decision taken at the network boundary guarantees the same switching behavior in each link of the routing path. As shown in Fig. 1 the network interface is augmented with an encoder and a decoder block. This technique is only concerned about the self-switching without disturbing the group switching. Note that the coupling capacitance in the state-of–the-art silicon technology is considerably larger compared with the self capacitance, and should be considered in any scheme proposed for the link power reduction.

PROPOSED ENCODING SCHEME

The proposed encoding scheme whose aim is to shrink power dissipation by minimizing the combination transition activities on the links of the interconnection network. The active power dissipated by the interconnect and drivers .The major goal of the future encoding scheme is to decrease the power dissipation by minimizing the coupling transition behavior on the links of the interconnection network. In they are classified four types of coupling transitions. A Type I occurs when one of the line is switches and remaining one is unchanged, Type II occurs when one of the lines switches from high to low and another one is switches from low to high, Type III occurs both the lines switches simultaneously, Type IV occurs when both the lines are remains unchanged.

Table 1: Effect of Odd and Even inversion on change of Transition Types

Time	Normal			Odd Inverted		
	Type I			Types II,III, and IV		
$t-1$	00,11	00,11,01,10	01,10	00,11	00,11,01,10	01,10
t	10,01	01,10,00,11	11,00	11,00	00,11,01,10	10,01
	T1*	T1**	T1***	Type III	Type IV	Type II
$t-1$	Type II			Type I		
t	01,10			01,10		
	10,01			11,00		
$t-1$	Type III			Type I		
t	00,11			00,11		
	11,00			10,01		
$t-1$	Type IV			Type I		
t	00,11,01,10			00,11,01,10		
	00,11,01,10			01,10,00,11		

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A. Scheme I

In scheme 1, our main target is to reducing the number of Type1 transitions and Type 2 transitions. Type 1 transitions is converted into Type III and Type IV transitions and Type II transitions is converted into Type I transitions. This scheme compares the two data's based on to reducing the link power reduction by doing odd inversion or no inversion operation.

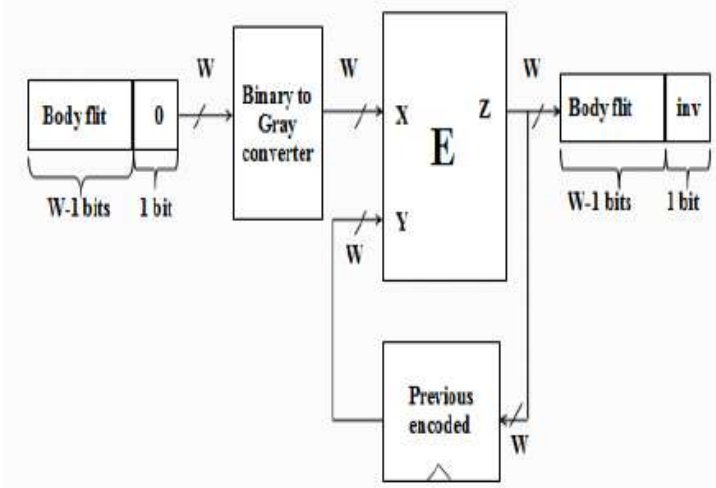

Fig 2. Scheme 1(a) Block diagram of encoder

The Fig2 shows the scheme-I encoder architecture. Here the TY block this takes two adjacent bits from the given inputs. From these two input bits the TY block checks what type of transitions occurs, whether more number of type 1 and type 2 transitions is occurring means it set the output state to 1, otherwise it set the output to 0. The odd inversion is performed for these types of transitions. Then the next block is the Majority code it checks the state, if the number of one's is greater than zeros or not and it implemented using a simple circuit. The last stage using the XOR circuits, this circuit is used to perform the inversion on odd bits. The decoding is performed by simply inverts the encoder circuit when the inverting bit is high

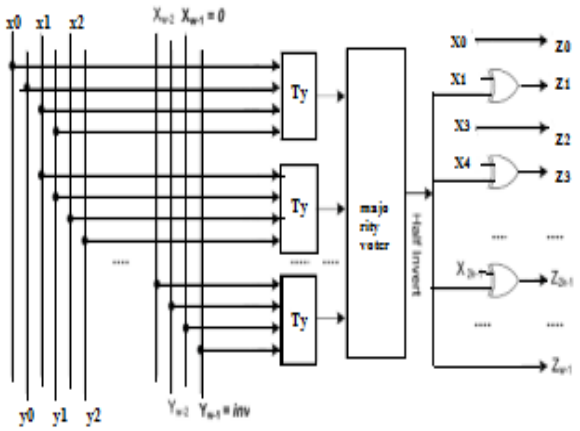

Fig 2. (b) Internal view of encoder

B. Scheme II

In scheme II, our main goal is to reducing the number of Type II transitions. Type II transitions are converted into Type IV transitions. This scheme compares the two data's based on to reducing the link power reduction by doing full 3sinversion or odd inversion or no inversion operation. Let us consider P odd, P full P even and P consume, as the power consumed by odd inversion, full inversion, even inversion and no inversion respectively. Amount of power consumed by the link when the input is even inverted is given by,

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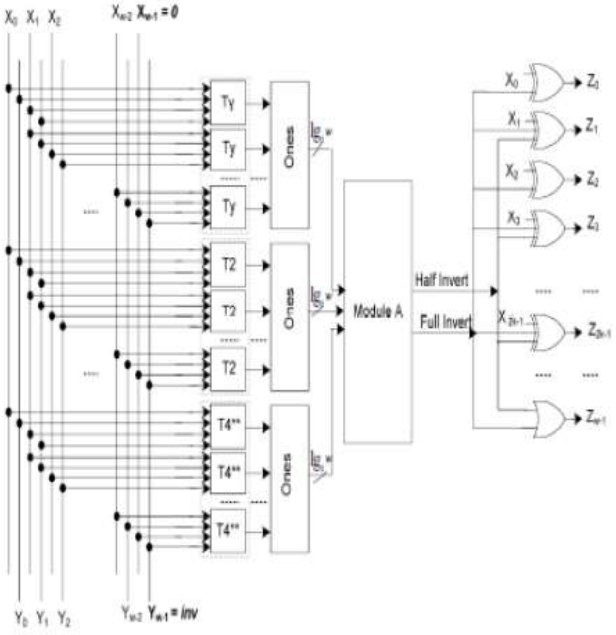

Fig 3. Scheme II Encoder architectures

Full and odd inversion based this advanced encoding architecture consist of w-1 link width and one bit for inversion bit which indicate if the bit travel through the link is inverted or not. W bits link width is considered when there is no encoding is applied for the input bits. Here the TY block from scheme 1 is added in scheme 2. This takes two adjacent bits from the given inputs. From these two input bits the TY block checks what type of transitions occurs. We have T2 and T4** blocks which determines if any of the transition types T2 and T4** occur based on the link power reduction. The number of one's blocks in the next stage. The output of the TY, T2 and T4** send through the number of one's blocks. The output of the ones block is log2w. The first ones block is used to determine the number of transitions based on odd inversion. The second ones block determines the number of transitions based on the full inversion and another ones block is used to determine the number of transitions based on the full inversion. These inversions are performed based on the link power reduction. Based on these ones block the Module A takes the decision of which inversion should be performed for the link power reduction. For this module is satisfied means the output is set to '1. None of the output is set to '1, if there is no inversion is takes place. The module A is implemented using full adder and comparator circuit.

DECODER

The block diagram of the decoder is shown in Fig 4. The w-1 bits input is applied in the decoder circuit and another input of the decoder is previous decoded output. The decoder block compares the two input data and inversion operation is performed and w-1 bits output is produced. The remaining one bit is used to indicate the inversion is performed or not. Then the decoder output is given to the gray to binary block. This block converts the gray code into original binary input.

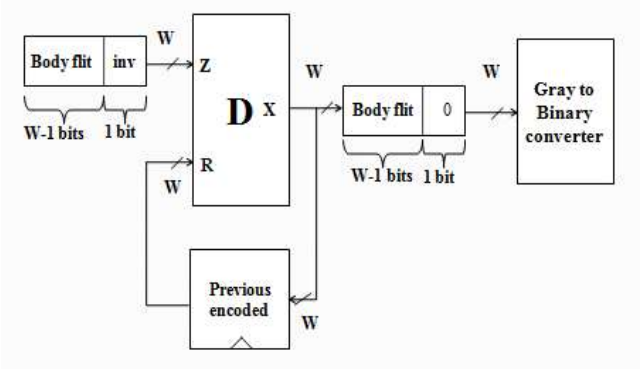

Fig 4. Block diagram of Decoder architecture

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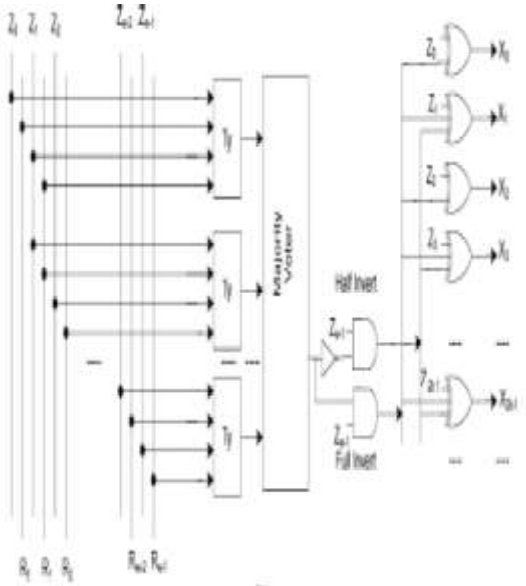

Fig 5. Internal View of Decoder

In decoder circuit diagram (Fig.5.) consist of TY block and Majority vector and XOR circuits. Based on the encoder action the TY block is determined the transitions. Based on the transitions types the majority blocks checks the validity of the inequality. The output of the majority voter is given to the XOR circuit. Half inversion, full inversion and no inversion is performed based on the logic gates.

C. Scheme III

In scheme III, calculation the even inversion into scheme II. The odd inversion converts Type I transitions into Type II transitions. From table converted into Type IV/Type III transitions by the flits is even inverted. The link power fall in even inversion is bigger than the Odd inversion.

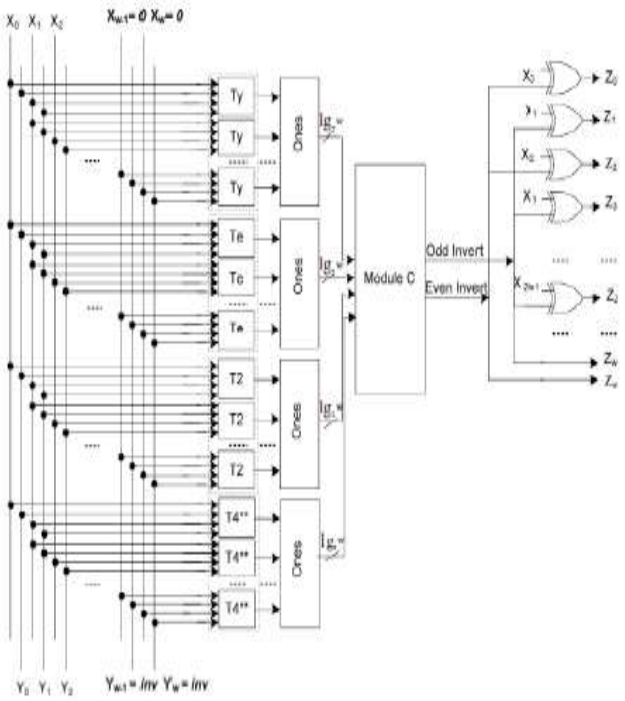

Fig 6. Scheme III of encoder architecture

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The encoding architecture (Fig.6) in scheme III is same of encoder architecture in scheme I and II. Here calculation the Te block to the scheme II. This is based on even invert state, odd invert condition and Full invert condition. It consists of w-1 link width input and the w bit is used for the inversion bit. The half, full and even Inversion is performed way the inversion bit is set '1', or else it set as '0'.The TY, Te and T4** block determines the transition types T2, Te and T4**. The transition types are throw to the number of one's block. The Te block is determined if some of the detected transition of types T2, T1** and T1***. The ones block determines the number of ones in the equivalent transmissions of TY, T2, Te and T4**. These numbers of one's is given to the Module C block. This block check if odd, even, full or no invert action corresponding to the outputs '10', '01', '11' or '00' correspondingly, should be performed. The decoder architecture of scheme II and scheme III are same.

SIMULATION AND RESULT

The encoder and decoder technique is implemented using a data scheme technique. The output waveform of encoder and decoder scheme shown in .The power consumption of existing system

Fig 7.scheme I output

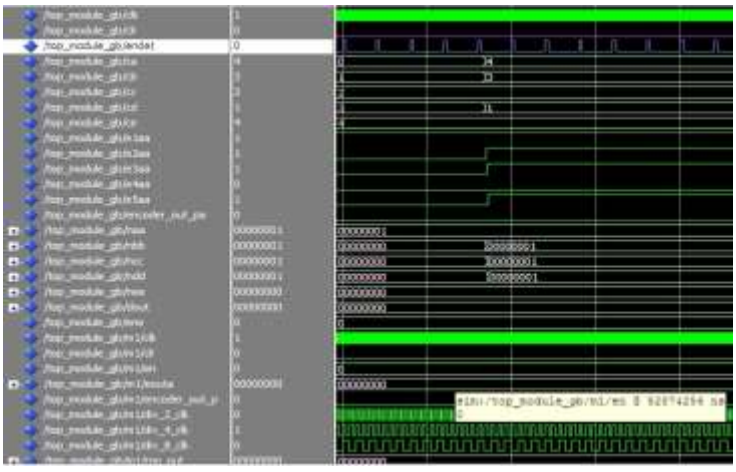

Fig 7.scheme II output

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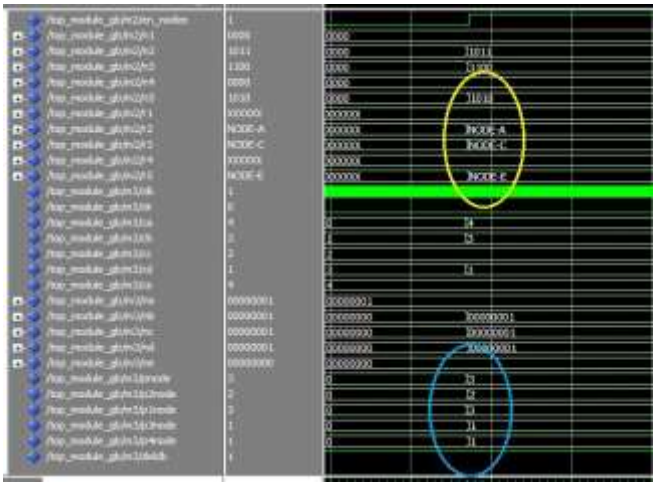

Fig 8.scheme III output

Table 2: power comparison table

S.no	Scheme	Power(mw)
1	Existing scheme	2.9
2	Scheme I	2.5
3	Scheme II	2.2
4	Scheme III	2.2

CONCLUSION

In this paper a new data encoding technique which allows dipping the power dissipated by the links of a NoC and contributed by both the pairing switching activity and the self switching activity. The encoder to decrease the number of transition .Gray code encoding method is used reduce the errors & noise. The proposed Encoding and Decoding techniques are used to reduce more than 20%of power dissipation. The proposed architecture is coded using VERILOG language and is simulated and synthesized using Modelsim or Xilinx software.

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