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DESIGN AND IMPLEMENTATION OF CARRY SELECT ADDER USING KOGGE-STONE TECHNIQUE

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ABSTRACT
In VLSI System design digital adder with optimum power is one of the important area of research. For many data processing purpose CSA perform fast air thematic function. So, it is clear that there is need to reduce the power consumption in CSA. This paper discusses about to reduce the power dissipation in CSA for many applications. For reduction purpose we use one of the most important approaches, which are Kogge –stone configuration. The proposed design with Kogge-stone adder CSA has reduced power dissipation compared with CMOS technology CSA. The simulation performed using SPICE circuit simulation at 0.18µm technology node & 1.8v standard CMOS process. This comparison with to CMOS logic in 10-100MHz transition frequency shows significant power saving.

INTRODUCTION
There are three sources of power dissipation in a digital complementary metal-oxide-semiconductor (CMOS) circuit. The first sources are the logic transitions. As the “nodes” in a digital CMOS circuit transition back and forth between the two logic levels, the parasitic capacitance are charged and discharged. Current flows through the channel resistance of the transistors, and electrical energy is converted into heat and dissipated away [1]. Short -circuit currents that flow directly from supply voltage to ground when the n-sub network and p-sub network of a CMOS gate both conduct simultaneously are the second source of power dissipation [1]. Both of the above sources of power dissipation in CMOS circuits are related to transitions at gate outputs and are therefore collectively referred to as dynamic dissipation. The third and last source of dissipation is the leakage current that flows when the inputs or outputs of a gate are not charging [1]. The CSA circuit has large power dissipation due to which it is not efficiently used in many VLSI techniques. For the application purpose there is need to reduce the power dissipation , for which we use Kogge-stone Adder in proposed circuit which reduces the power dissipation as compared to CMOS CSA circuit. This paper has been divided into five sections. The section I describes the power dissipation in CMOS logic. Section II describes the circuit description and working of CSA and Kogge-stone adder. Section III describes the proposed work in which carry select adder is implemented by using Kogge-stone adder to save the power in VLSI techniques. Section IV & V are all about simulation result and conclusion respectively.

CIRCUIT DISCRIPTION
Carry select adder
It composed of two four-bit ripple carry adder per section. Both Sum and Carry bit are calculated for the two alternatives of the input carry “0”and”1”. The carry out of each section, which then selects the appropriate ripple carry adder .The very first section, has a carry-in of zero [2]. Fig 1 shows an example of 4-bit carry select adder.
Kogge-stone adder
KSA is a parallel prefix from carry look ahead adder. It generates carry in o (logn) time and is widely considered as the fastest adder and widely used in the industry for high performance air thematic circuit [3]. Kogge –stone is 12 times faster than a standard ripple carry adder [4]. An example of 4-bit Kogge-stone is shown in Fig 2. A generate and proposed signal are created in the first stage that are than used to compute the intermediate carrier in parallel. The final sum is as XOR of the carry and proposed signals [4].
It can be divided into three distinct parts-

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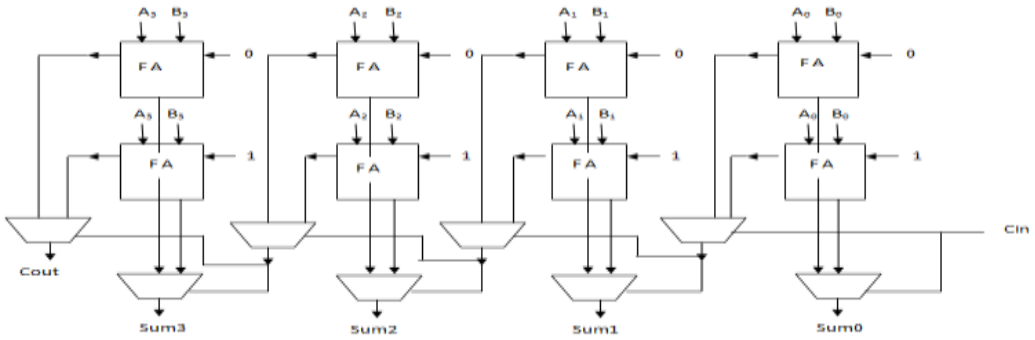


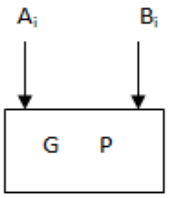
Fig 1 .4-bit Carry Select Adder

A. Pre Processing

This step involves computation of generate and propagate signals corresponding too each pair of bit in A and B. These signals are given by the logic equations below [4]

$P=A_i$ XOR B_i (Propagate Signal)……(i)

$G=A_i$ AND B_i (Generate Signal)……. (ii)

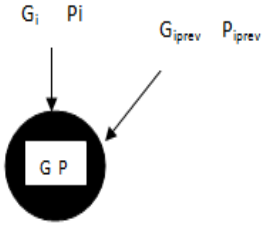


B. Carry look ahead adder

This block differentiate KSA from other adders and is the main force behind its high performance. This step involves computation of carriers corresponding to each bit. It uses group propagate and generate as intermediate signals which are given by the logic equation below [4].

$P=P_i$ AND P_{iprev}…….(iii)

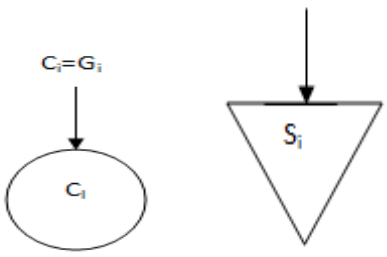
$G=G_i$ OR (P_i AND G_{iprev})…….(iv)



Post Processing

This is the final step and is common to all adders of this family. it involves computation of sum bits . Sum bits are computed by the logic given below [4]

$S_i=P_i$ XOR C_{iprev}……. (v)



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An example of 4-bit Kogge-stone adder shown in Fig 2. The total of stages used in any Kogge-stone adder is calculated by (logn) where n=no of input bits. From LSB to MSB we can observe the in each stage the black nodes are shifted to 2^{l-1} (Where l=stage numbers) horizontally and reduced black nodes are replaced with white nodes. The black nodes are reduced finally to n/2 (where n=no of input bits).

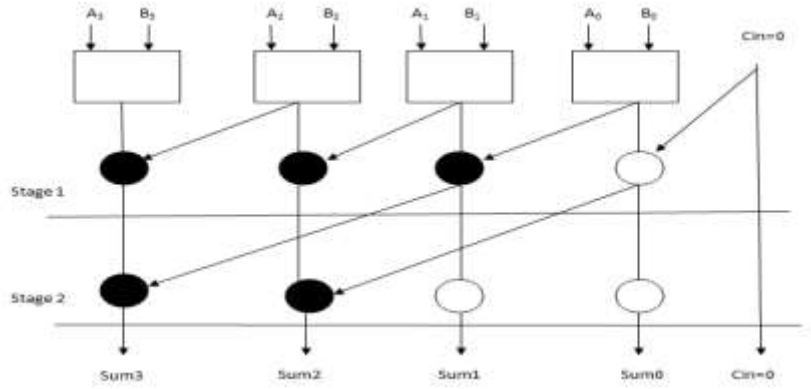

Fig2. 4-bit Kogge-Stone Adder

PROPOSED WORK

In proposed work I have implemented a carry select adder using 1-bit Kogge-stone adder, Fig 2 shows 1-bit Kogge-stone adder through which a full adder with Cin=0 is replaced by it, which reduces the power dissipation for the complete circuit. Fig 3 shows Carry select adder with Kogge-stone adder (at Cin=0).

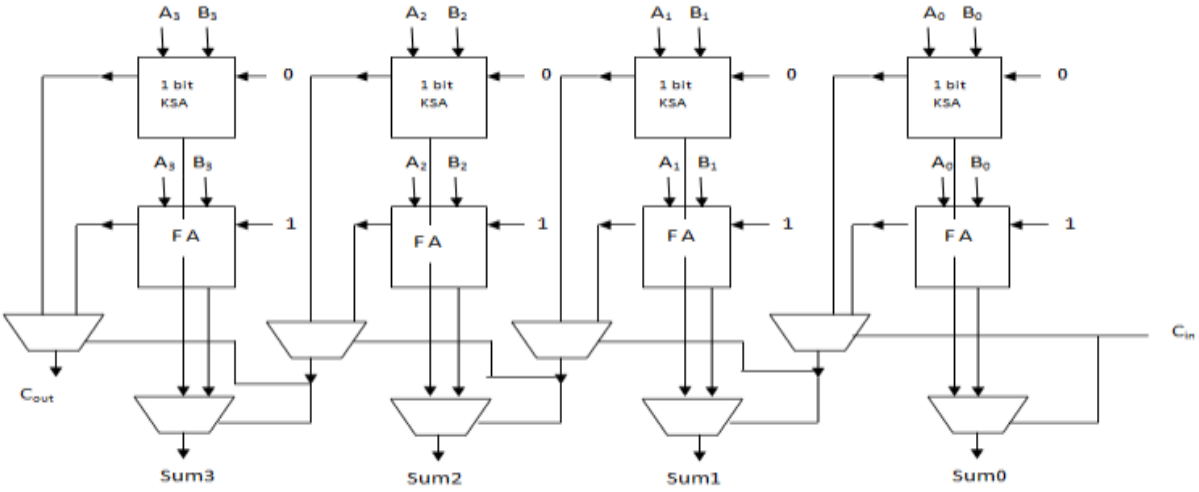

Fig 3. Proposed Carry Select Adder with Kogge-Stone Adder (at Cin=0)

SIMULATION RESULT AND DISSCUSION

Fig 4, 5 and 6 shows the output waveforms of proposed circuit for 4, 8 or 6 bits respectively.

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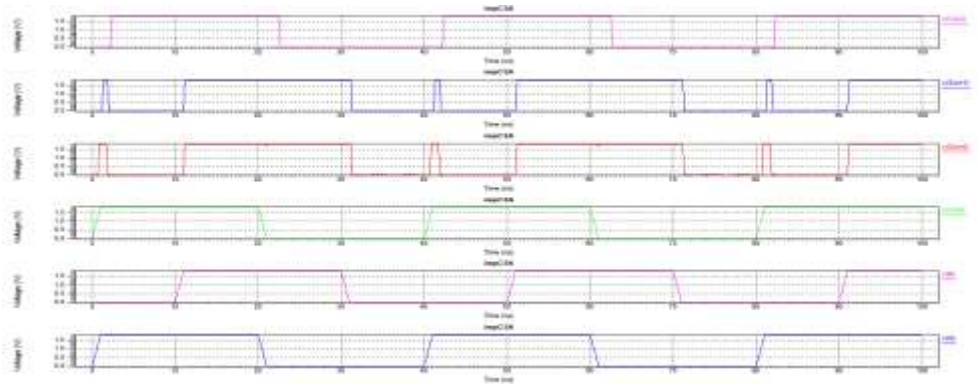

Fig4. Output Waveform of 4-bit proposed CSA

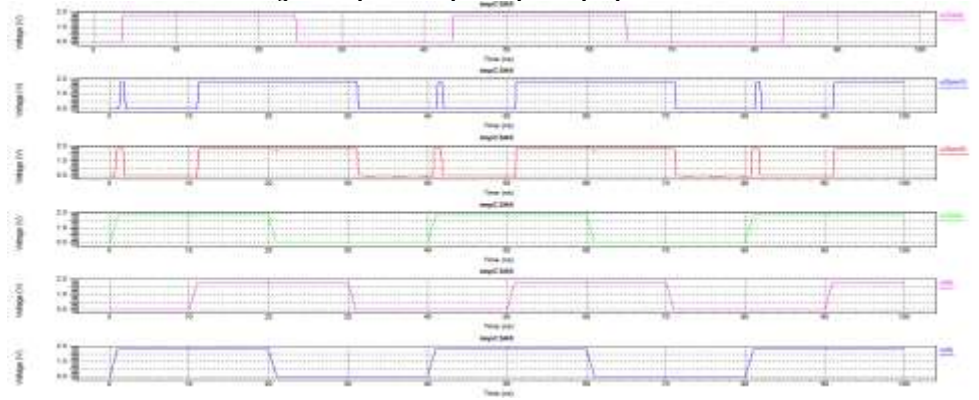

Fig5.Output Waveform of 8-bit proposed CSA

From Fig 7, 8 and 9 it may observe that as voltage increases, power dissipation of all circuits increases but CMOS technology based CSA have larger power dissipation at each voltage in comparison to proposed CSA (PCSA). In other side from fig 10,11 and 12 as frequency increases power dissipation of both circuits increases (CMOS technology based CSA Vs Proposed CSA) Whereas proposed circuit have lesser power dissipation at each frequency in comparison to convention CMOS.

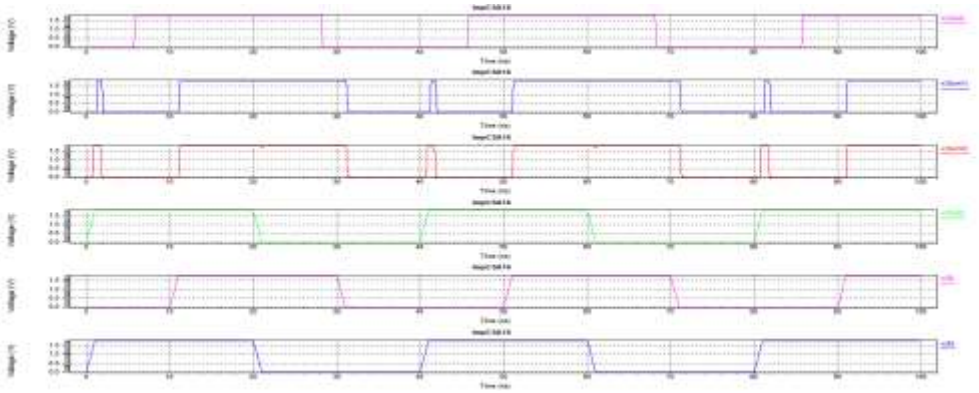

Fig6. Output Waveform of 16-bit Proposed CSA

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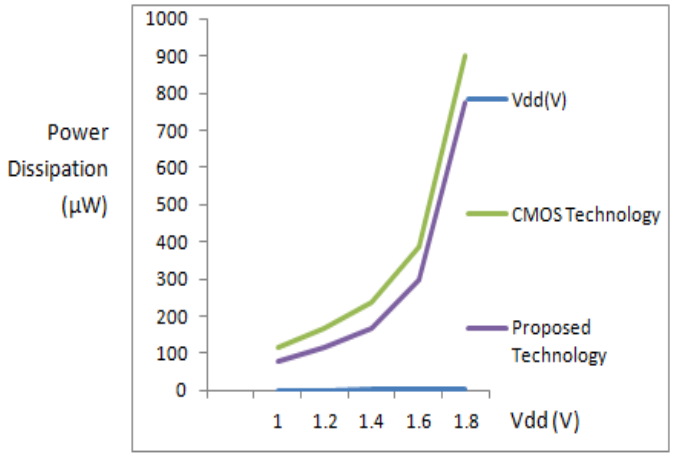

Fig7. Power Dissipation of Both technologies for 4-bit CSA at different voltages

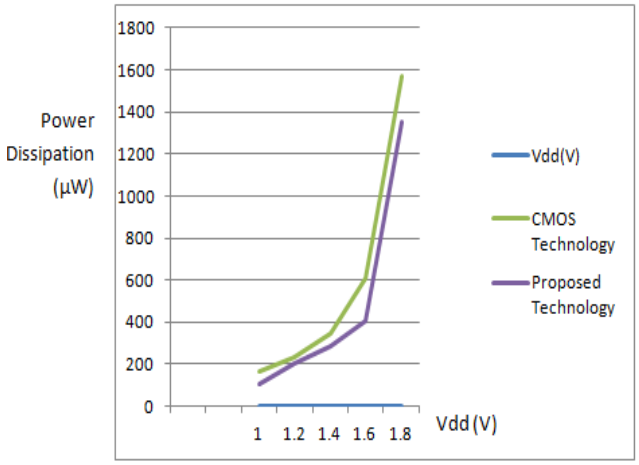

Fig8. Power Dissipation of Both technologies for 8-bit CSA at different voltages

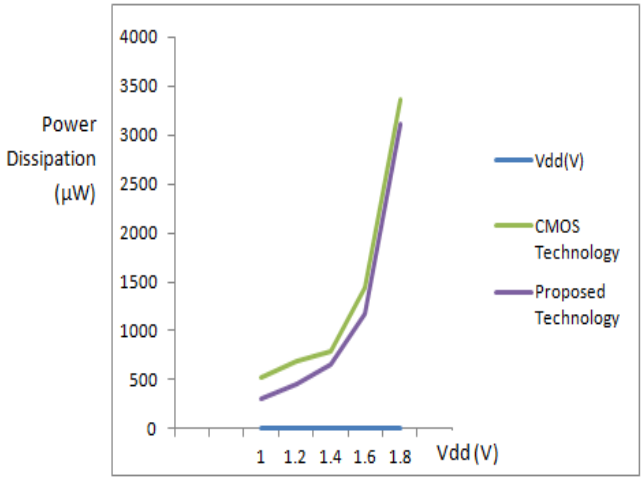

Fig9. Power Dissipation of Both technologies for 16-bit CSA at different voltages

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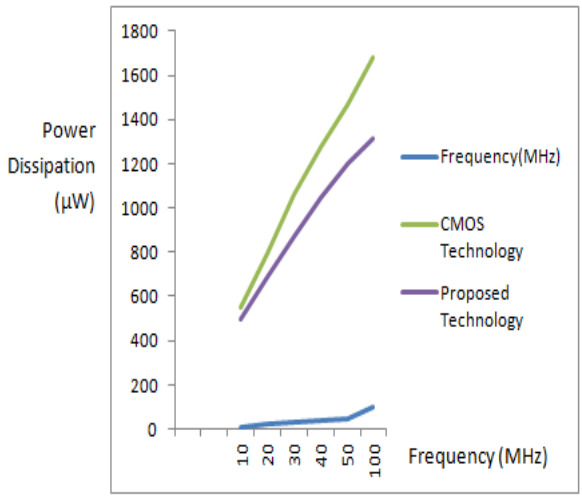

Fig10. Power Dissipation of Both technologies for 4-bit CSA at different frequencies

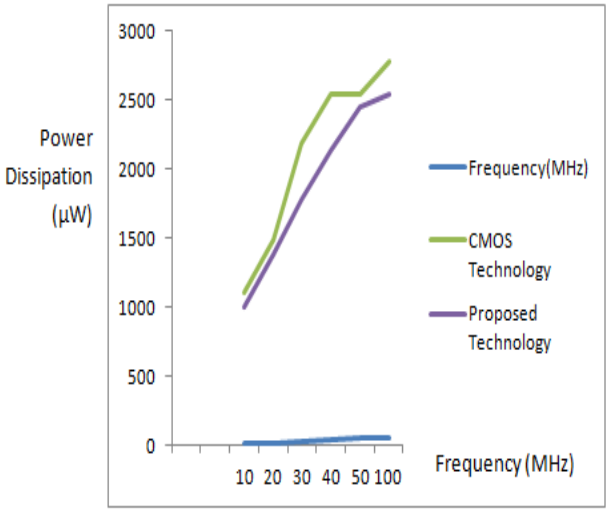

Fig11. Power Dissipation of Both technologies for 8-bit CSA at different frequencies

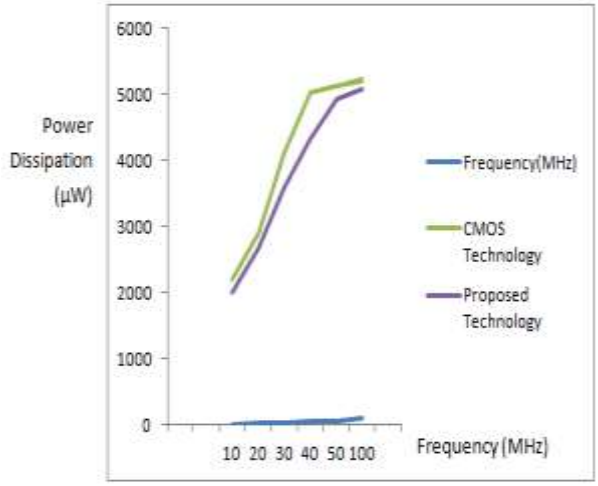

Fig12. Power Dissipation of Both technologies for 16-bit CSA at different frequencies

Table no 1 and 2 shows the comparative study between both circuits for 4,8or16 bits respectively in term of voltage Vs power dissipation or frequency Vs power dissipation.

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Table 1 Comparative study between Voltage Vs Power dissipation for both Technologies of 4, 8or 16 bit CSA

Vdd(V)	4-bit CSA		8-bit CSA		16-bit CSA	
	CMOS technology	Proposed technology	CMOS technology	Proposed technology	CMOS technology	Proposed technology
1	116.8026	78.1523	162.2553	105.5901	516.0227	315.1463
1.2	168.784	114.5513	235.485	204.5974	684.7663	457.7046
1.4	236.1136	166.6983	343.4537	289.2973	790.5275	659.6034
1.6	387.1886	297.8531	610.2477	409.1361	1443.678	1180.907
1.8	898.9178	773.1523	1569.59	1351.089	3363.441	3102.452

Table 2 Comparative study between Frequency Vs Power dissipation for both Technologies of 4 ,8 or 16 bit CSA

Frequency (MHz)	4-bit CSA		8-bit CSA		16-bit CSA	
	CMOS technology	Proposed technology	CMOS technology	Proposed technology	CMOS technology	Proposed technology
10	551.1609	494.222	1102.695	1000.546	2214.091	2003.243
20	797.2472	683.9387	1493.599	1389.94	2903.145	2682.765
30	1065.215	873.231	2185.383	1778.799	4095.869	3590.965
40	1274.96	1047.199	2539.089	2137.719	5032.96	4320.313
50	1462.802	1198.056	2543.276	2447.786	5140.837	4937.389
100	1678.609	1312.675	2785.567	2541.321	5223.652	5076.321

CONCLUSION

The comparison of proposed circuit with other traditional methodologies has proved that power consumption with the proposed logic is less as compared to CMOS based techniques for CSA (at 4, 8 or 16 bits). Therefore it is clear that by using the above proposed circuit we have save the power and efficiently used it in low power VLSI techniques.

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