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A SURVEY ON A HIGH SPEED BINARY FLOATING POINT MULTIPLIER USING DADDA ALGORITHM IN FPGA

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ABSTRACT

In Digital Signal Processing, Floating Point (FP) Multiplication is widely used in large set of scientific and signal processing computation. Multiplication is one of the common arithmetic operations in these computations. Most of the DSP applications need floating point numbers multiplication. The possible ways is to represent real numbers in binary floating point numbers format. The IEEE 754 standard represents two floating point formats, Binary interchange format and Decimal interchange format resp. The main object of this paper is to reduce the power consumption and to increase the speed of execution for multiplying two floating point number using FPGA.

INTRODUCTION

Floating point numbers are one possible way of representing real numbers in binary format; the IEEE 754 standard presents two different floating point formats, Binary interchange format and Decimal interchange format. Multiplying floating point numbers is a critical requirement for DSP applications involving large dynamic range. Floating-point implementation on FPGAs has been the interest of many researchers. FPGAs are increasingly being used in the high performance and scientific computing community to implement floating-point based hardware accelerators. FPGAs are generally slower than their application specific integrated circuit (ASIC) counterparts, as they can't handle as complex a design, and draw more power. However, they have several advantages such as a shorter time to market, ability to re-program in the field to fix bugs, and lower nonrecurring engineering cost costs. Vendors can sell cheaper, less flexible versions of their FPGAs which cannot be modified after the design is committed. The Development of these designs is made on regular FPGAs and then migrated into a fixed version that more resembles an ASIC.

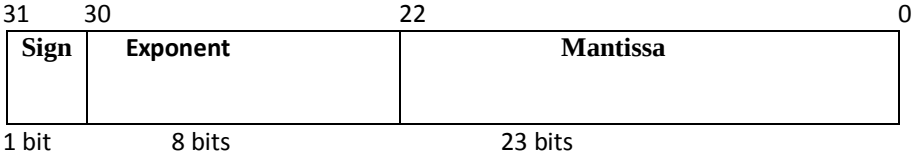

Fig1.Single Precision Floating point format

The Single-precision number is 32-bit wide. The single-precision number has three main fields that are sign, exponent, and mantissa .The 24-bit mantissa can approximately represents a 7-digit decimal number, while an 8-bit exponent to an implied base of 2 provides a scale factor with a reasonable range. Thus a total of 32-bit is needed for single-precision number representation.

This paper presents a high speed binary floating point multiplier based on Dadda Algorithm. The coding is done for 32-bit single precision floating point multiplication using VHDL. Our method using Dadda method can have a great impact on improving the speed and reduce the area and power consumed by the Digital Signal Processors. The design achieves high speed with maximum frequency compared to existing floating point multipliers. The floating point multiplier is developed to handle the underflow and overflow cases.

LITERATURE REVIEW

Various researches have been done to increase the performance on getting best and fast multiplication result on two floating point numbers. Some of which are listed below-

Addanki Puma Ramesh, A. V. N. Tilak, A.M.Prasad [1] the double precision floating point multiplier supports the LEEE-754 binary interchange format. The design achieved the increased operating frequency. The implemented design is verified with single precision

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floating point multiplier and Xilinx core, it provides high speed and supports double precision, which gives more accuracy compared to single precession. This design handles the overflow, underflow, and truncation rounding mode resp.

Itagi Mahi P and S. S. Kerur [2] ALU is one of the important components within a computer processor. It performs arithmetic functions like addition, subtraction, multiplication, division etc along with logical functions. Pipelining allows execution of multiple instructions simultaneously. Pipelined ALU gives better performance which will evaluated in terms of number of clock cycles required in performing each arithmetic operation. Floating point representation is based on IEEE standard 754. In this paper a pipelined Floating point Arithmetic unit has been designed to perform five arithmetic operations, addition, subtraction, multiplication, division and square root, on floating point numbers. IEEE 754 standard based floating point representation has been used. The unit has been coded in VHDL. The same arithmetic operations have also been simulated in Xilinx IP Core Generator.

Remadevi R [3] Multiplying floating point numbers is a critical requirement for DSP applications involving large dynamic range. This paper presents design and simulation of a floating point multiplier that supports the IEEE 754-2008 binary interchange format, the proposed multiplier does not implement rounding and presents the significant multiplication result. It focuses only on single precision normalized binary interchange format. It handles the overflow and underflow cases. Rounding is not implemented to give more precision when using the multiplier in a Multiply and Accumulate (MAC) unit.

Rakesh Babu, R. Saikiran and Sivanantham S [4] A method for fast floating point multiplication and the coding is done for 32-bit single precision floating point multiplication using Verilog and synthesized. A floating point multiplier is designed for the calculation of binary numbers represented in single precision IEEE format. In this implementation exceptions like infinity, zero, overflow are considered. In this implementation rounding methods like round to zero, round to positive infinity, round to negative infinity,
round to even are considered. To analyse the working of our designed multiplier we designed a MAC unit and is tested.

These results are compared with the previous work done by various authors.

Gargi S. Rewatkar [5] FPGAs are generally slower than their application specific integrated circuit (ASIC) counterparts, as they can't handle as complex a design, and draw more power. However, they have several advantages such as a shorter time to market, ability to re-program in the field to fix bugs, and lower non-recurring engineering costs. Vendors can sell cheaper, less flexible versions of their FPGAs which cannot be modified after the design is committed. The development of these designs is made on regular FPGAs and then migrated into a fixed version that more resembles an ASIC. In this paper the aim was to implement double precision floating point multiplier in VHDL. Double precision floating point multiplier implemented in VHDL may be used applications such as digital signal processors, general purpose processors and controllers and hardware accelerators.

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Ref.No.	Name of Researcher(s)	Topic	Date of Publication	Method	Outcome of research
1	A.P.Ramesh, A.V.N. Tilak, A.M.Prasad	An FPGA Based High Speed IEEE-754 Double Precision Floating Point Multiplier U sing Verilog	Mar-13	Double precision, Floating point, Multiplier, FPGA,IEEE-754	This design handles the overflow, underflow, and truncation rounding mode
2	Itagi Mahi P and S. S. Kerur	Design and Simulation of Floating Point Pipelined ALU Using HDL and IP Core Generator	March - April 2013	ALU, IEEE standard 754, Single Precision, Pipelining, Hardware Description Language (HDL), VHD	The pipelined Floating point Arithmetic unit has been designed to perform all arithmetic operations on floating point numbers
3	Remadevi R	Design and Simulation of Floating Point Multiplier Based on VHDL	March - April 2013	Floating point multiplication, VHDL simulation	proposed multiplier doesn‟t implement rounding and presents the significand multiplication result
4	A. Rakesh Babu, R. Saikiran and Sivanantham S.	Design of Floating Point Multiplier for Signal Processing Applications	Volume 8, Number 6 (2013)	32-bit single precision floating point format; Dadda Algorithm; Floating point.	This multiplier is designed and simulated using Xilinx ISE v13.4.
5	Gargi S. Rewatkar	Implementation of Double Precision Floating Point Multiplier in VHDL	Apr-13	Floating Point Multiplier, FPGA, VHDL.	may be used as digital signal processors, general purpose processors and controllers and hardware accelerators.

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6	P.Gayatri, P.K.Kumari, V.V.Krishna, T.S.Trivedi, V.Nancharaiah	Design of Floating Point Multiplier Using Vhdl	Mar-14	Floating point number, Exponent, Mantissa, Normalization, rounding, Overflow	The floating point multiplier is design for both 32-bit and 64-bit by varying the input variables

CONCLUSION

The main focus of this paper is to introduce a method for calculating the multiplication of two floating point numbers with comparatively lesser time. It describes an implementation of a floating point multiplier that supports the IEEE 754- 2008 binary interchange format. The multiplier is more precise and it presents the significant best multiplication result. It may be used applications such as digital signal processors, general purpose processors and controllers and hardware accelerators etc. The implemented design is also efficient in terms of device utilization .The idea proposed here may set path for future research in this direction. Future scope of research this is to reduce area requirements and can be extended to various fields of DSP.

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